REMARKS

Prior to entry of this amendment, claims 1-18 are pending. By this amendment, a substitute specification is presented. The specification is amended to correct errors of a typographical nature. A clean version of the specification and a marked-up version showing changes to the specification are attached. No new matter is added.

Corrected drawing Figs. 2 and 3 are presented as Replacement Sheets. No new matter is added by the amendments to the drawings.

Also by this amendment, claims 2, 5 and 10 are cancelled and claims 1, 3, 4, 6, 9, 11 and 14 are amended. No new matter is added by the amendments to the claims. Therefore, claims 1, 3, 4, 6-9, and 11-18 are pending and subject to Examination.

Favorable reconsideration of this application is respectfully requested in view of the foregoing amendments and following remarks.

Objections to the Specification and Drawings

In the Office Action mailed December 3, 2004, the drawings are objected to for typographical errors. Presented herewith are replacement sheets of Figs. 1, 2 and 3, in which typographical errors have been corrected. Applicants respectfully request withdrawal of the objection to the drawings.

The specification is objected to for numerous occurrences of use of the word "designation" in place of - -destination- -. A substitute specification is presented herewith, in which all occurrences of "designation" have been replaced with - -destination- -. A marked-up version of the specification showing changes made thereto is also attached, in which additions are represented by underlining and strike-through

indicates deletions. No new matter is added. Applicants respectfully request withdrawal of the objection to the specification.

Claims 1, 4, 7-9 and 12-18 Recite Patentable Subject Matter

Claims 1, 4, 7-9 and 12-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,633,973 to Kanzaki (hereinafter, "Kanzaki"). It is noted that claims 1, 4, 9, and 14 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

Independent claims 1, 4, 9, and 14 recite a method, a device or a system for information processing, each having, among other features and/or steps, a feature in which an absolute branching destination address is received and stored in a buffer circuit, a flag is generated based on the absolute branching destination address, a relative branching destination address is generated based on the stored absolute branching destination address, and either one of the absolute branching destination address and the relative branching destination address is outputted based on the flag. In addition, each of claims 1, 4, 9, and 14 includes a feature wherein, when the absolute branching destination addresses fully occupy the buffer circuit, a predetermined absolute branching destination address stored in the buffer circuit is deleted, and the flag, which is associated with the absolute branching destination address subsequent to the address deletion, is shifted to output the absolute branching destination address when the flag, which is associated with the absolute branching destination address subsequent to the address deletion, indicates the output of the relative branching destination address.

Applicants respectfully submit that Kanzaki neither discloses nor suggests all of the features of the invention as recited in independent claims 1, 4, 9 and 14. For example, Kanzaki neither discloses nor suggests deleting a predetermined absolute branching destination address stored in the buffer circuit when the absolute branching destination addresses fully occupy the buffer circuit. Further, Kanzaki neither discloses nor suggests shifting the flag, which is associated with the absolute branching destination address subsequent to the address deletion, to output the absolute branching destination address from the output unit when the flag, which is associated with the absolute branching destination address subsequent to the address deletion, indicates the output of the relative branching destination address, as recited in the claimed invention.

Rather, Kanzaki discloses at col. 7, line 35 – col. 8, line 6, a CPU 2 outputting a control signal requesting execution of a branch instruction. A selector circuit 33 determines, based on the control signal outputted from the CPU 2, whether the address outputted by the CPU 2 is a branching source address or a branching destination address. When a branching source address is outputted, the branching source address latch 35 latches the branching source address. When the branching destination address is outputted, the branching destination latch 37 latches the branching destination address. These values are written in a memory 43 via a selector 42.

Kanzaki does not disclose or suggest deleting a predetermined absolute branching destination address when the absolute branching destination addresses fully occupy the buffer circuit. Kanzaki similarly fails to disclose or suggest shifting the flag, which is associated with the absolute branching destination address subsequent to the

address deletion, to output the absolute branching destination address when the flag, which is associated with the absolute branching destination address subsequent to the address deletion, indicates the output of the relative branching destination address.

To establish *prima facie* obviousness of a rejected claim, the applied art of record must teach or suggest each feature of a rejected claim. *See M.P.E.P. §2143.03.* As explained above, Kanzaki neither discloses nor suggests each and every feature recited in independent claims 1, 4, 9 and 14. Accordingly, Applicants respectfully submit that Kanzaki neither anticipates nor renders obvious the present invention as recited in independent claims 1, 4, 9 and 14.

For at least the reasons set forth above, Applicants respectfully submit that independent claims 1, 4, 9 and 14 are patentably distinct over Kanzaki and in condition for allowance.

Each of claims 3, 6-8, and 11-18 depends from one of claims 1, 4, 9 and 14. Therefore, Applicants respectfully submit that claims 3, 6-8, and 11-18 are allowable for the same reasons as claims 1, 4, 9 and 14, as well as for the additional subject matter recited therein.

Accordingly, withdrawal of the rejection of claims 1, 4, 7-9 and 12-18 under 35 U.S.C. § 103(a) is respectfully requested.

Claims 3, 6 and 11 Recite Patentable Subject Matter

Claims 2, 3, 5, 6, 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanzaki in view of U.S. patent No. 5,809,293 to Bridges et al. (hereinafter, "Bridges"). It is noted that claims 2, 5 and 10 have been canceled, and claims 3, 6, and 11 have been amended to depend from independent claims 1, 4 and 9,

respectively. To the extent that the rejection remains applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

As explained above, Kanzaki does not disclose or suggest deleting a predetermined absolute branching destination address when the absolute branching destination addresses fully occupy the buffer circuit. Kanzaki similarly fails to disclose or suggest shifting the flag, which is associated with the absolute branching destination address subsequent to the address deletion, to output the absolute branching destination address when the flag, which is associated with the absolute branching destination address subsequent to the address deletion, indicates the output of the relative branching destination address.

Applicants respectfully submit that Bridges similarly fails to disclose or suggest shifting the flag, which is associated with the absolute branching destination address subsequent to the address deletion, to output the absolute branching destination address when the flag, which is associated with the absolute branching destination address subsequent to the address deletion, indicates the output of the relative branching destination address as recited in each of independent claims 1, 4, 9 and 14.

Rather, Bridges discloses at col. 4, line 18 – col. 5, line 10, detecting a trace event by the event detection logic 106 and selectively outputting a branch target address from the link register 108, a loop count from the count register 109 that can be decremented during execution of branch instructions, and a current instruction address from the instruction address register 110 via the MUX 114, the FIFO 102 and the trace serialization logic 115. Moreover, Bridges discloses at col. 7, lines 48-50, when the FIFO 102 is full, a value FIFO_FULL is transmitted to control logic 103 to stall

processing within the microprocessor 100. This is not the same as shifting the flag, which is associated with the absolute branching destination address subsequent to the address deletion, to output the absolute branching destination address when the flag, which is associated with the absolute branching destination address subsequent to the address deletion, indicates the output of the relative branching destination address as recited in each of independent claims 1, 4, and 9.

Since neither Kanzaki nor Bridges, alone or in combination, discloses or suggests the invention as recited in independent claims 1, 4, and 9, it is respectfully submitted that claims 1, 4, and 9 are patentably distinct over the combination of Kanzaki and Bridges, and in condition for allowance.

Claims 3, 6 and 11 depend from claims 1, 4, and 9, respectively. Thus, Applicants respectfully submit that claims 3, 6 and 11 are allowable for the same reasons as claims 1, 4, and 9, as well as for the additional subject matter recited therein.

Accordingly, withdrawal of the rejection of claims 3, 6, and 11 under 35 U.S.C. § 103(a) is respectfully requested.

Conclusion

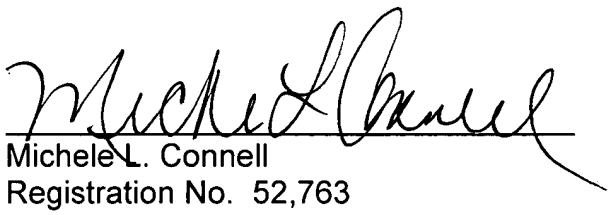
For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

Arent Fox PLLC



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Enclosure: Petition for Extension of Time
Clean Version of Substitute Specification
Marked-up Version of Substitute Specification
2 Replacement Sheets